Mody University of Science and Technology
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"Analytic Modeling of Low-dimensional Nano-Scale Semiconducting Devices"

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Research Proposal

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1. Introduction

Solid state materials with reduced dimension in one or two or three directions are recognized as low dimensional materials. Based on reduced dimension, the low dimensional materials are in generally classified as 2D, 1D and 0D, and are shown in Fig.1.1. Bulk materials is called as 3D materials, Due to reduced dimension, electron motion in the materials is restricted either in one or two or three directions.

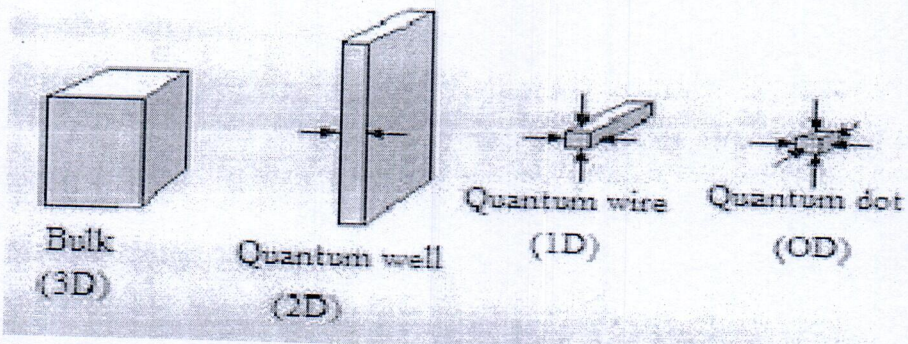

Fig.1.1 Schematic representation of various forms of low dimensional materials

Quantum Confinement

In nanomaterial's, the electronic energy levels are not continuous as in the bulk but are discrete. This is due to the electrical confinement of the electronic wave function in one, two or three physical dimensions of the materials and accordingly it can be classified as

- 1D confinement – Thin film, Quantum well
- 2D confinement – Nanotubes, Quantum wire
- 3D confinement - Quantum dots

Electronic Properties

The electronic properties changes occur in the low dimensional material are related to the wave like property of the electron and scarcity of the scattering centers. As the size of the system becomes comparable with the de Broglie wavelength of the electrons, the discrete nature of the energy states becomes occur as shown in Fig. 1.2. In certain cases, conduction material becomes insulator below the critical length scale.

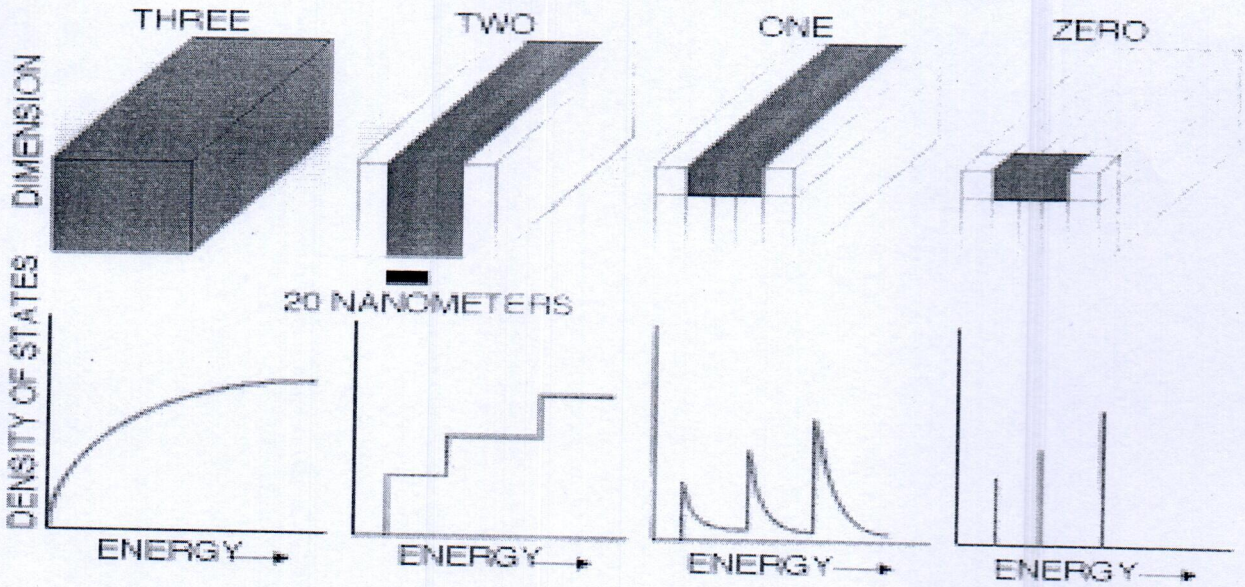

Fig.1.2 Density of states variation with 3D, 2D, 1D and 0D material

1.1 Theory of Low Dimensional Semiconductor Devices

As a spatial dimension approaches the atomic scale, a transition occurs from the classical laws to the quantum-mechanical laws of physics. Phenomena that occur on the atomic or subatomic scale cannot be explained outside the framework of quantum-mechanical laws.

In quantum mechanics, the trajectory of a moving particle loses its meaning when the distance over which potential energy varies is on the order of the de Broglie wavelength:

$$\lambda = \frac{2\pi}{\sqrt{2mE}}\hbar \qquad (1)$$

where $\hbar$ is the reduced Planck constant, m is the mass of the particle, and E is its energy.

The quantum effects of confinement become significant when at least one of the dimensions of a structure is comparable in length to the deBroglie wavelength. If at least one dimension of a solid is comparable to the de Broglie wavelength of the particle, a quantum-mechanical treatment of particle motion becomes necessary. In the Schrödinger description of quantum mechanics, an elementary particle e.g., an electron, a hole and a photon—or even a physical system such as an atom is described by a wave function $\Psi(r\,t)$, which depends on the variables describing the degrees of freedom of the particle (system). The square of the wave function is interpreted as the probability of finding a particle at spatial location $r = (x, y, z)$ and time t.

The wave function of an uncharged particle with no spin satisfies the Schrödinger wave equation which takes the following form in semi-classical approach.

$$\left(-\frac{\hbar^2}{2m}\nabla^2 + V(\vec{r},t)\right)\Psi(\vec{r},\mathrm{t}) = E\Psi(\vec{r},\mathrm{t}) \qquad (2)$$

where$\nabla^2 = \frac{\partial^2}{\partial x} + \frac{\partial^2}{\partial y} + \frac{\partial^2}{\partial z}$ is the Laplacian operator, V($\vec{r}$ t) is the varying potential influencing the particle's motion. For a particle (electron or hole) in a solid, this mass is its effective mass m, which is usually less than the mass of an isolated electron. In the above equation the action of Hamiltonian operator,

$$H(\vec{r},t) = -\frac{\hbar^2}{2m}\nabla^2 + V(\vec{r},t) \qquad (3)$$

yields total energy of the particle i.e. kinetic energy + potential energy. The first part is of hamiltonian operator $-\frac{\hbar^2}{2m}\nabla^2$ gives kinectic energy and second part $V(\vec{r},t)$gives potential enery of the particle. For many real systems, the potential does not depend on time, ie$V(\vec{r},t) = V(r)$.Using this representation of the wave function in the Schrödinger equation, the time harmonic Schrödinger equation is obtained and can be written as,

$$\left(-\frac{\hbar^2}{2m}\nabla^2 + V(\vec{r})\right)\Psi(\vec{r}) = E\Psi(\vec{r}) \qquad (4)$$

Analytical solutions of the time-harmonic Schrödinger equation can be obtained for a variety of relatively simple conditions. These solutions provide an insight into the nature of quantum phenomena and sometimes provide a reasonable approximation of the behavior of more complex systems—e.g., in statistical mechanics, molecular vibrations are often approximated as harmonic oscillators. Several of the more common analytical solutions are for a free (isolated) particle: a particle in a box, a finite potential well, 1D lattice etc.

For example let the length of the box be L with infinite potential barrier at the distance x=0 and x=L and let an electron of mass m be represented by the wave function ψ(x) can be equated as,

$$H\psi = E\psi \qquad (5)$$

where H is Hamiltonian and E is total energy (sum of potential and kinetic energy) also it is allowed eigen values (energies) of the electron in the orbital (i.e., here the study is for a system of single electron and the orbital model is valid only if when there is no interactions between electrons)

As the total energy considered is mainly kinetic equation takes the form

$$H = \frac{P^2}{2m} \qquad (6)$$

where P is the momentum, and is equal to $-i\hbar\frac{d}{dx}$

Solution to this problem leads to allowed energies values in the box and it takes form as

$$E_n = \frac{\hbar^2}{2m}(k^2) \qquad (7)$$

Where k is propagation vector given as $\frac{n\pi}{L}$ and n is an integer. The fig. 1.3 represents variation of E with k. And E takes discrete values.

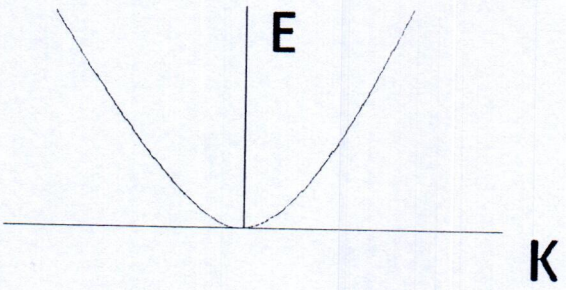

Fig.1.3 Allowed energies E vs Propagation Vector K

1.1.1 Energy Band formation

Following the Kronig-Penney model, understanding of energy bend formation can be realized. In the model the array of one dimensional atoms is taken, there potential variation is approximated as series of wells shown in the fig 1.4

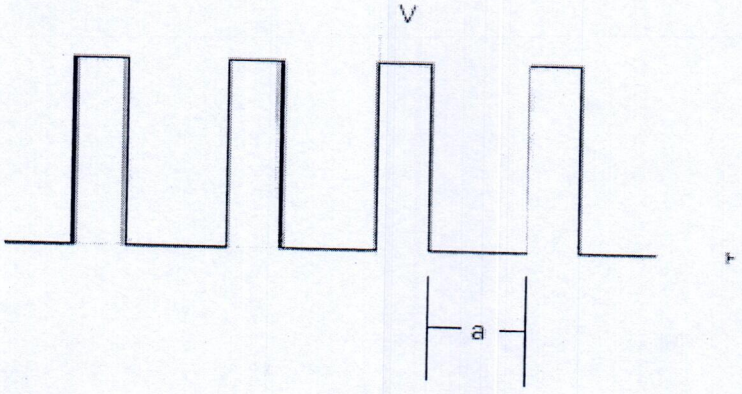

Fig. 1.4 Potential variation V for series of 1D atoms with 'a' as interatomic spacing

As the interatomic spacing is reduced to less than the length of a well, the interaction between atoms increase and the allowed energy solution take very large values as shown in Fig. 1.5

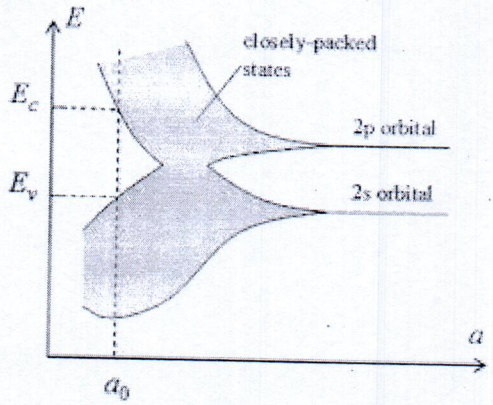

Fig. 1.5 Energy band formation

1.1.2 Density of States

Density of states for electron is nothing but the number of available energy states for the electron to occupy. Knowledge about this helps us to understand the electronic transport phenomena. Let it be denoted as $\rho(E)$ and this is dealt with in the energy range of E and $E + dE$ with the representation as $\rho(E)dE$.
The density of states for a quantum well for conduction band is given as

$$\rho_c(E) = \frac{m_c}{\hbar\pi L_z} \tag{8}$$

Where m_c is effective mass of electron in conduction band and L_z is length of the semiconductor in z direction.
The density of states helps us to calculate the number of available states N that electrons or hole can take. And thus the total carrier concentration which is given as

$$n(in\ conduction\ band) = \int_{E_c}^{\infty} \rho(E) f(E) dE \tag{9}$$

where f(E) is occupation probability, given as

$$f\ (E) = \frac{1}{1 + e^{[(E-E_f)/kT]}} \tag{10}$$

1.2Quantum Structures

1.2.1 Quantum Well

The term "well" refers to a semiconductor region that is grown to possess a lower energy; so that it acts as a trap for electrons and holes (electrons and holes gravitate towards their lowest possible energy positions). They are referred to as "quantum" wells because these semiconductor regions are only a few atomic layers thick; in turn, this means that their properties are governed by quantum mechanics, allowing only specific energies and band gaps. Because QW structures are very thin, they can be modified very easily. In other words Quantum wells are real-world implementation of the "particle in the box" problem; they act as potential wells for charge carriers and are typically experimentally realized by epitaxial growth of a sequence of ultrathin layers consisting of semiconducting materials of varying composition.

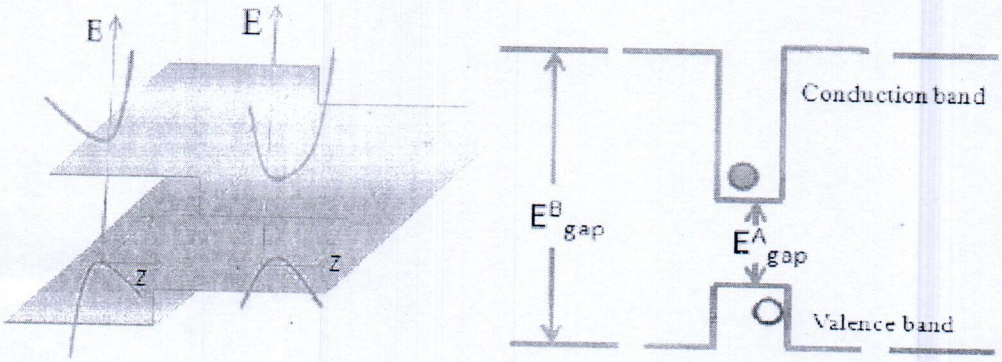

Fig.1.6 Energy band formation in the quantum well structures

Two dissimilar semiconductors with different band gaps can be joined to form a heterojunction. The discontinuity in either the conduction or the valence band can be used to form a potential well. If a thin layer of a narrower-band gap material 'A' say, is sandwiched between two layers of a wider-band gap material 'B', then they form a double heterojunction. If layer 'A' is sufficiently thin for quantum properties to be exhibited, then such a band alignment is called a single quantum well.

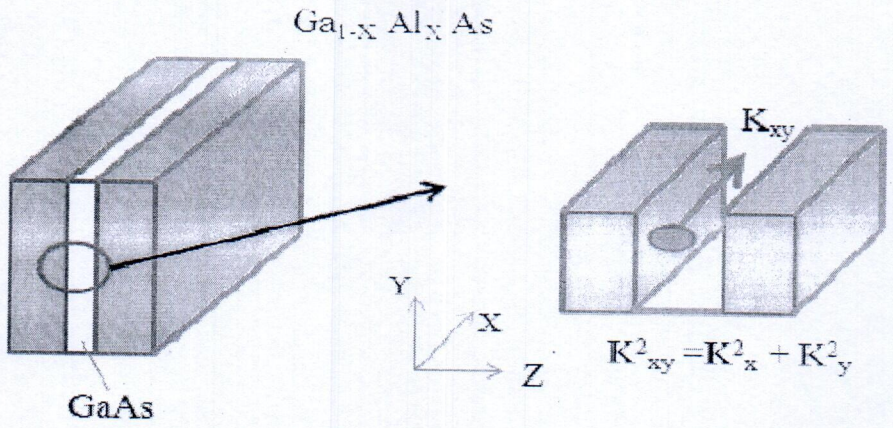

Fig. 1.7 Quantum well formation

1.2.2 Quantum Wire

A standard quantum well layer can be patterned with photolithography or perhaps electron-beam lithography, and etched to leave a free standing strip of quantum well material; the latter may or may not be filled in with an overgrowth of the barrier material (in this case, $Ga_{(1-x)}Al_x\ As$). Any charge carriers are still confined along the heterostructure growth *(z-)* axis, as they were in the quantum well, but in addition (provided the strip is narrow enough) they are now confined along an additional direction, either the *x-* or the y-axis, depending on the lithography.

The following Fig. shows an expanded view of a single quantum wire, where clearly the electron (or hole) is free to move in only one direction, in this case along the y-axis.

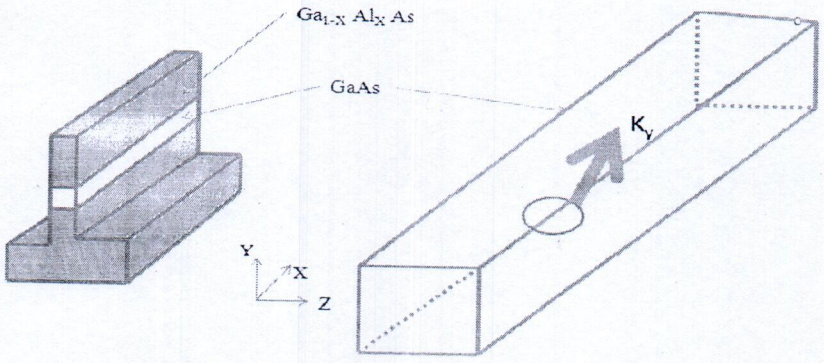

Fig. 1.8 Quantum wire formation

1.3Challenges to CMOS technology

Complementary metal-oxide-semiconductor (CMOS) technology scaling has been a main key for continuous progress in silicon-based semiconductor industry over the past three decades. However, as the technology scaling enters nanometer regime, CMOS devices are facing many serious problems such as increased leakage currents, difficulty on increase of on-current, large parameter variations, low reliability and yield, increase in manufacturing cost, and etc. To sustain the historical improvements, various innovations in CMOS materials and device structures have been researched and introduced. In parallel with those researches, various new nanoelectronic devices, so called "Beyond CMOS Devices," are actively being investigated and researched to supplement or possibly replace ultimately scaled conventional CMOS devices. While those nanoelectronic devices offer ultra-high density system integration, they are still in a premature stage having many critical issues such as high variations and deteriorated reliability. The practical realization of those promising technologies requires extensive researches from device to system architecture level.

Issues for nanoscale MOSFETs:

- *Sub-threshold leakage current*
- *Threshold voltage variation*
- *Carrier mobility degradation*
- *Hot carrier effects (HCEs)*
- *Direct source to drain tunneling*
- *Direct tunneling gate leakage current*
- *Gate depletion*
- *Parasitic resistance*
- *Parasitic capacitance*
- *Reverse-biased junction leakage current*

As the device scaling is approaching its physical size limitations, the technology cycle is getting slow down due to increasing power consumption, process variation, and fabrication cost. To continue the historical growth for the next decade, various studies have been conducted to overcome ever increasing challenges. Nowadays device scaling tradeoffs between performance and power consumption, therefore technological innovations which can achieve high performance through very low power are required. These efforts have made conventional MOSFETs evolve in various ways with new materials, new structures, and so on. In the next section, the evolution of MOSFET structures is reviewed.

1.4Future Scope

The conventional device scaling trend, which is mostly based on reducing its physical size, is no longer valid for the future technology generations. Therefore, several strategies have been introduced to extend Moore's Law, such as increasing electrostatic control over the channel by means of the continued EOT scaling with high-k/metal gate stack and multi gate structures for higher drive current at constant over- drive voltage (VDD-Vth), improving mobility of carriers by adopting high mobility channel materials and strain engineering, reducing parasitics, and so on.

1.4.1 Silicon on Insulator (SOI)

The advantages of SOI technology come from its buried oxide (BOX) layer (a cross section of a SOI device is shown in Fig. 1.9). With the reduction of the parasiticcapacitances, mostly as a result of the reduceddrain/source junction capacitances, SOI devices yieldimproved switching speed and reduced powerconsumption. The operating speed is also improved sincethe isolated channel from substrate bias prevents theincrease in a threshold voltage of stacked SOI transistors.In addition, the perfect lateral and vertical isolation fromsubstrate provides latch-up and inter-device leakage freeCMOS technology, reduction in various interferences, and better soft error immunity. Moreover, SOI technologyoffers tighter transistor packing density and simplified processing.

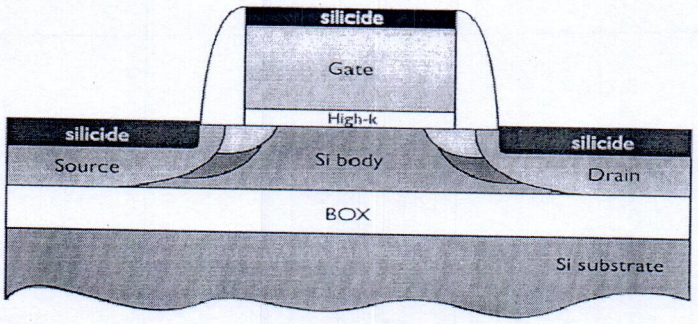

Fig. 1.9 SOI MOSFET

There are two types of Partially Depleted SOI and Fully Depleted SOI MOSFETs Another important merit of SOI technology is that it provides the cornerstone for new device structures such as multi gate field-effect transistors (MuGFETs), which includes more than one gate into a single device.

1.4.2 Double Gate MOSFET

The double-gate (DG) MOSFET shown in Fig. 1.10 is the first step for those multi gate devices. Since the transverse electric field induced by $V_{DS}$is shared by both top and bottom channels, it mitigates SCEs. However, since the gate-channel-gate stacked structure is not suitable for Si planar technology to fabricate, the complex fabrication processes are required to form DG FETs. These problems are considerably eased with a self-aligned FinFET as shown in the Fig. 1.10.

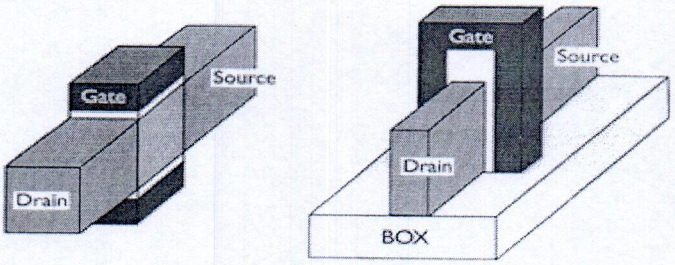

Fig.1.10 DG-MOSFET and FinFET

Better scalability can be achieved by introduction of a second gate at the other side of the body of each transistor resulting in a double-gate SOI structure. Due to the excellent control of the short channel effects, double-gate SOI devices have emerged as the device of choice for circuit design in sub-50 nm regime Low sub threshold leakage and higher ON-current in the double-gate devices make them suitable for circuit design in sub-50 nm regime . One of the promising structures in the double-gate technology is FinFET due to the simple fabrication process. Double-gate devices with isolated gates (independent gates) are being developed. The independent gate option can be useful for low power and mixed signal applications. Such developments at the device level provide opportunities for new ways of circuit design for low power and high performance. ITRS reports also show the inevitable inclusion of DGMOSFETs in upcoming VLSI applications.

Advantages of DG MOSFETs

- Nearly ideal subthreshold slope.
- Small intrinsic gate capacitance
- Smaller junction capacitances.
- Better immunity to SCEs, although negligible for subthreshold operation.
- Reduced Random dopant fluctuations (RDF) due to undoped or lightly doped body and reduced carrier mobility degradation.
- Higher ION/IOFF ratio.
- Design flexibility at circuit level by symmetric/asymmetric with tied and independent gate options.

1.4.2 Gallium-Nitride (GaN) Based High Electron Mobility Transistor (HEMT)

High output power at high frequencies is required in wireless communication (satellite communications, TV broadcasting, broadband wireless internet connection, transmitter base station amplifiers) and military applications (radars, missile seekers). The typical III-V semiconductors (As-based) achieved significant success in optoelectronic devices, i.e LEDs, LDs, with a wide spectral range, and High Electron Mobility Transistors (HEMT). But growing requirement for higher output power generation in case of RF requires new semiconductor materials and device designs. A variety of power amplifier technologies with different materials of suitable band-gap are vying for market share, such as GaAs (or GaAs/InGaP) hetero-junction bipolar transistors (HBT) and HEMTs, SiC MESFETs, and GaN HEMTs [4]. Some of the material properties of various contenders are listed in Table 1.1.

Table 1.1 Different Properties of Various materials

Semiconductor Material		Si	GaAs	SiC	GaN
Characteristics	Unit				
Band gap	eV	1.1	1.42	3.25	3.49
Electron Mobility	$Cm^2/V\text{-}s$	1500	8500	700	2000(2DEG)
Saturated electron velocity	Cm/s	10^7	$1.3x10^7$	$2.0x10^7$	$2.1x10^7$
Critical breakdown field	MV/cm	0.3	0.4	3.0	3.0

In addition to large band-gap and higher JM (Jhonson's figure of Merit), the polar nature of the GaN crystal gives it an edge over other materials. The crystal polarization in GaN and AlGaN leads to the formation of charged interfaces. This results in accumulation of electrons and holes near the interface. Piezo-electric polarization in nitrides has been found to be ten times higher than in arsenides. These two charge accumulation mechanisms result in very high polarization based electron density in GaN-based hetero-structures very near to the interface. This 2 Dimensional Electron Gas (2DEG) forms even without any significant doping. The absence of doping and spatial separation of channel electrons from ionized donors leads to the reduction of ionized impurity scattering and, consequently, an

increase in electron mobility. The resulting 2DEG density in GaN-based devices has been reported to be around and, in many cases, above $10^{13}cm^{-2}$, making it almost six times larger than that of a GaAs HEMT. A higher mobility and electron density leads to higher output current density. Nowadays, the reported output power density of 30-40 W/mm is more than ten times higher than that of GaAs based transistors. Thus, for the same output power, device size can be reduced by the same factor using GaN.

Advantages of GaN - based HEMT

- The high output power density allows the fabrication of much smaller size device with the same output power.
- Higher impedance due to smaller size allows for easier and lower loss matching in amplifiers.
- The operation at high voltage due to its high breakdown electric field not only reduces the need for voltage conversion, but also provides the potential to obtain high efficiency which is a critical parameter for amplifiers.
- The wide bandgap also enables it to operate under high temperature. At the same time, the HEMT topology gives device better noise performance than that of MESFET topology.
- In conclusion, the high carrier concentration, the high electron saturation velocity and the large breakdown voltage make GaN-based HEMT a very promising candidate for microwave power applications.

Formation and Structure of 2DEG GaN HEMT

A hetero-structure is formed when two different materials are joined together or grown one over the other keeping the same crystal structure. When such a hetero-junction is formed between two materials having a large band gap difference, an energy discontinuity is created in the band diagram shown in the figure.

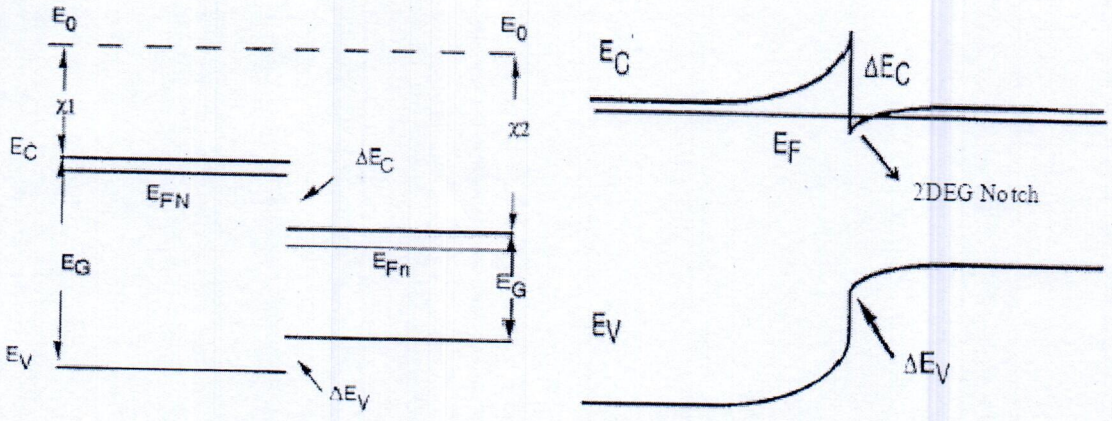

Fig.1.11 Band Gap Diagram for 2DEG HEMT

But In case of III-Nitride based devices, the principle behind the formation of 2DEG is basically different from that in conventional hetero-structures described above. In III-N based heterostructures, the dominant cause behind the accumulation of carriers at the interface is inherent net polarization, resulting in interface charge without the presence of any significant doping which further enhances their mobility.

A HEMT is very similar to a Field Effect Transistor in the sense that the current flowing between the source and drain terminals (ohmic contacts) is controlled by the electrical field generated by the voltage applied at the gate terminal (Schottky barrier) perpendicular to the current direction as shown in Fig.. Electrons flow in the channel formed by the 2DEG region.

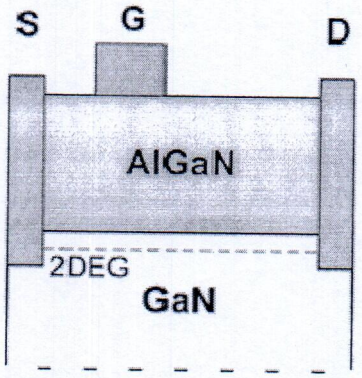

Fig.1.12 AnAlGaN/GaN HEMT structure.

2 Literature Review

There is immense research going on multiple gate field effect transistors. Due to scaling challenges under sub-10nm regions, newer structures needs to thoroughly looked into. The broader areas over which research on multiple gate field effect transistors are as follows

a) Modeling the Channel Charge and Potential in Quasi-Ballistic Nanoscale Double-Gate MOSFETs [1-3]
b) Threshold voltage modeling of Double-Gate MOSFETs[3, 11]
c) Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors[5,6]
d) Semi analytical Model of the Subthreshold Current in Short-Channel Junctionless Symmetric Double-Gate Field-Effect Transistors [6-7]
e) A Short-Channel Common Double-Gate MOSFET Model Adapted to Gate Oxide Thickness Asymmetry[6-7,11,13]
f) On-current modeling of short-channel double-gate (DG) MOSFETs [12,13]
g) A surface-potential based model for GaN HEMTs in RF power amplifier applications [14-16]
h) High-Performance GaN-Based Nanochannel FinFETs With/Without AlGaN/GaN Heterostructure [17-20]
i) High-Performance Junctionless MOSFETs for Ultralow-Power Analog Applications [1-4]

3 Research Proposal

3.1 Compact modeling of Double gate MOSFETs

A two dimensional semi-analytical solution for the surface potential for junctionless/with junction symmetric double-gate field effect transistors in subthreshold regime, which is based on the parabolic approximation for the potential is being investigated. With this an analytical expressions for the threshold voltage and subthreshold slope with quantum confinement effects will be derived. Based on such a solution, a semi-analytical expression for the current will be derived. The potential and current models are validated through comparisons with TCAD simulations and are used to evaluate relevant short-channel effect parameters, such as threshold roll-off, drain-induced barrier lowering, and inverse subthreshold slope

3.2 Current modeling for Double gate MOSFET and FinFETs

An analytical drain current model will be derived for doped short-channel double-gate MOSFETs and FinFETs with a Gaussian-like doping profile in the vertical direction of the channel. The model will be valid in linear and saturation regions of device operation. The drain current variation with various device parameters such as transconductance will be observed. Parameters like transconductance and drain conductance that are important in assessing the analog performance of the device will also be formulated.

3.3 High-Performance GaN-Based Nanochannel FETs With/WithoutAlGaN/GaN Heterostructure

Two types of field-effect transistors (FETs), one with AlGaN/GaN heterojunction and the other with heavily doped heterojunction-free GaN layer operating in junctionless mode will be compared interms of their transport properties. Their ON/OFF current ratio will be calculated. The proposed GaN Nanochannel FETs are very promising candidate's notonly for high performance, but also for high power applications.

3.4 Analytical modeling of AlGaN/GaN Based HEMT

An analytical model based on surface potential that include parasitic capacitances will be developed for RF GaN HEMTs. It will be expected that such an approach will be superior to other modeling techniques in terms of scalability and model performance for applications where accurate distortion modeling is of paramount importance. By introducing parasitic components, the capacitances for the full structure of the HEMT devices will be given. Meanwhile, the effects of bulk traps and surface traps in the capacitances are analyzed. The complete model, including currents and capacitances has been implemented in i-MOS platform for evaluations and circuit simulations.

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